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Harmonic Analysis and Mitigation of Low-Frequency Switching Voltage Source Inverter with Auxiliary VSI

Haofeng Bai, *Member, IEEE*, Xiongfei Wang, *Senior Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*, Poh Chiang Loh

Abstract— The output currents of high-power Voltage Source Inverters (VSIs) are distorted by the switching harmonics and the background harmonics in the grid voltage. This paper presents an active harmonic filtering scheme for high-power, low-frequency switching VSIs with an additional auxiliary VSI. In the approach, the auxiliary low-power, high-frequency switching VSI is used to compensate both the switching harmonics of the high-power VSI and the low-order harmonics introduced by the distorted grid voltage. Impedance modeling and analysis are implemented for the hybrid VSI system, where the impacts of the grid impedance are analyzed. Different control targets are then formulated based on the analysis, and the corresponding control strategies are proposed. Lastly, simulations and experimental results are provided to validate the theoretical analysis and the performance of the proposed control strategy.

Index Terms— voltage source inverter; LC filtered VSI; impedance model

I. INTRODUCTION

HIGH-power Voltage Source Inverters (VSIs) are widely used in large scale renewable power generation and AC motor drives [1]–[3]. The output current of the high power VSIs are often polluted by both the switching harmonics and the low order harmonics introduced by the distorted grid voltage. In order to reduce the switching harmonics in the output current, passive filters, such as the LCL or LLCL filters, are often used [23], [28]. The cross-over frequency of the passive filters should be well below the switching harmonics and yet above the current control bandwidth [18], [19], [23]–[25]. For the high power VSIs with low pulse-ratio, it is not trivial to design the passive filters. The current control bandwidths of the high power VSIs are also limited by their low pulse-ratio and the corresponding low crossover frequencies of the filters [3]. The lack of the current control

bandwidth in turn results in the sensitivity to the grid background harmonics [4], [5]. By adopting multiple-sampling techniques, the current control bandwidth can be improved [6]. However, the switching ripples can be introduced into the control system. Frequency-selective current control techniques are also proposed for L filters with well-designed Proportional and Resonant (PR) controllers to push targeted frequencies of the current control loop [7]. Nevertheless the performance of the improved PR controller can be impaired by the lower crossover frequency of the high order filters. What is more, VSIs equipped with the passive filters always suffer from the stability issues brought by the variance of the grid impedance [8], [12].

Integration of the well-established Active Power Filtering (APF) technologies with the high power VSI seems a feasible option for high power DC/AC conversion. Hybrid power conversion system composed of a lined commutated converter (LCC) and an APF has been proposed and investigated [9], [10]. The LCC is responsible for the bulk of power of the system, while the APF compensates for the low-order harmonics brought by the LCC. Since the power rating of the APF is lower compared with the LCC, the switching frequency can be higher, which allows easy design of the passive filters. However, this kind of power conversion faces several shortcomings: 1) the LCC can not operate without the APF due to the high magnitude of the low order harmonics, 2) the performance of the APF is dependent on the grid-impedance [11]. Other hybrid power conversion systems consisting of a high-power VSI with low pulse-ratio and a low-power Current Source Inverter (CSI) with high switching frequency have also been proposed and investigated [13]–[17]. The challenge for switching harmonic filtering of the high power VSI with a common VSI based APF is that its current control bandwidth should be much higher than the traditional APFs. Since the output current of the CSI can be synthesized fast, the switching harmonics and the low order harmonics of the high power VSI can be compensated with lower control effort. The drawback of the hybrid power conversion system with CSI is that the dc-link inductor is heavy and additional diode rectifier is needed for protection issue.

Recently, an Active Trap Filter (ATF) based on a series LC filtered VSI is proposed to attenuate the switching harmonics of the high-power VSIs [17]. Instead of tracking the harmonic

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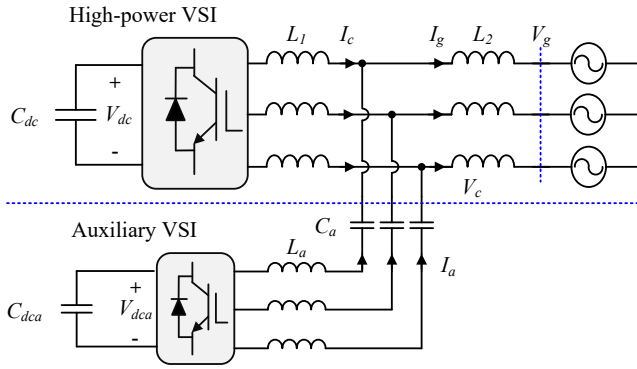


Fig. 1. System configuration of the power conversion system composed of a high-power VSI and a series LC filtered auxiliary VSI.

current reference, the ATF modifies its output impedance at the harmonic frequencies and provides a low-impedance path to by-pass the switching harmonics of the high power VSI. With the output impedance shaping method, the design of the current controller and the calculation of the current reference for the ATF are greatly simplified. The LC filter reduces the power rating and dc-link voltage of the auxiliary VSI compared to the L or LCL filter [16], [17]. The topology of the power conversion system composed of a high-power VSI and a series LC filtered VSI is shown in Fig. 1. The system in [17] is still sensitive to background harmonics in the grid voltage. Since the switching harmonics and the low order harmonics are introduced by different harmonics sources, they cannot be analyzed and compensated in the same manner.

The contribution of this paper is the derivation of an improved control system of the auxiliary VSI so that the grid current I_g remains sinusoidal even in the presence of grid harmonics. In order to achieve this target, the harmonics interaction within the system shown in Fig. 1 is analyzed considering the impedance model of the high power VSI and the series LC filtered VSI at the switching frequencies and the low order harmonics. Above the Nyquist frequency of the high-power VSI, the high-power VSI is represented by a harmonic voltage source; below the Nyquist frequency of the high power VSI, the normal Norton equivalent models are used for both the high-power VSI and the auxiliary VSI. Based on the impedance model, it will be shown in § III that the control targets and the resultant operation principles of the auxiliary VSI should be different in different frequency ranges. Instead of emulating a virtual impedance, the auxiliary VSI should compensate the harmonic current directly and increase its output impedance. The control strategies of the auxiliary VSI are proposed in § IV based on the control targets. The derived control system of the auxiliary contains three control loops to 1) compensate the switching harmonics of the high-power VSI, 2) compensate the low order harmonics introduced by the grid voltage and 3) maintain the dc-link voltage of the auxiliary VSI. Besides, it will be shown that the current control loops of the auxiliary VSI also introduce virtual resistance, which affects the stability of the system against the variation of the grid impedance. Also, the low order harmonics in the converter side current of the high-power VSI will increase with the grid impedance. The tuning

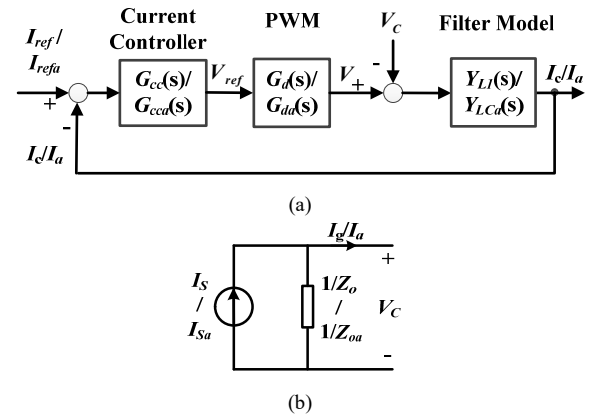


Fig. 2. Impedance model of the high-power VSI and the auxiliary VSI. (a). Current control diagram for the high-power VSI and the auxiliary VSI. (b). Norton equivalent circuit of the high-power VSI and the auxiliary VSI.

method of the control parameters is explained as well as simulation and experimental results are provided in § V and § VI. The conclusions are drawn in § VII.

II. IMPEDANCE MODEL AND HARMONIC DISTRIBUTION ANALYSIS

A. Impedance Model of the System

In the system shown in Fig. 1, the high-power VSI controls the converter side current I_c and the auxiliary VSI controls its output current I_a . The current control diagrams for the high-power VSI and auxiliary VSI are shown in Fig. 2(a). In the figure, I_{refg} is the current reference, G_{cc} is the current controller, G_d is the time delay of the current control loop of the high-power VSI, respectively. Y_{L1} is the admittance of the converter side inductor L_1 . I_{refa} , G_{cca} and G_{da} are the counter parts of the auxiliary VSI and Y_{Lca} is the admittance of the series LC filter. Based on the current control diagrams, both the high-power VSI and the auxiliary VSI can be represented by their impedance models which are composed of an ideal current source and the paralleled output impedance [20]–[22], [26]. The impedance models are shown in Fig. 2(b). In the figure, I_s is the current source and Z_o is the output impedance of the high-power VSI, which includes the effect of the converter side inductor L_1 and the current control loop. The expressions of I_s and Z_o can be obtained by (1) and (2).

$$I_s = I_{refg} \frac{G_{cc} G_d}{G_{cc} G_d + L_1 s} \quad (1)$$

$$Z_o = G_{cc} G_d + L_1 s \quad (2)$$

I_{sa} and Z_{oa} are the current source and output impedance of the auxiliary VSI, respectively. The expressions of I_{sa} and Z_{oa} can be obtained by (3) and (4).

$$I_{sa} = I_{refa} \frac{G_{cca} G_{da}}{G_{cca} G_{da} + L_a s + 1/C_a s} \quad (3)$$

$$Z_{oa} = G_{cca} G_{da} + L_a s + \frac{1}{C_a s} \quad (4)$$

Since the impedance models are based on the average model of the VSIs, they are valid only below their Nyquist frequencies and both of the impedance models are valid below the Nyquist frequency of the high-power VSI. Hence they are in this paper used for the analysis of harmonic interaction introduced by the distorted grid voltage. The impedance model of the system below the Nyquist frequency of the high-power VSI is shown in Fig. 3. Z_{L2} is the impedance of the grid side inductor L_2 . The distorted grid voltage is represented by a harmonic voltage source V_h and V_g is the ideal grid voltage.

As indicated by (1) and (2), I_s contains only the fundamental component and Z_o reflects the disturbance rejection ability of the current control loop of the high-power VSI. Since the ideal voltage source V_g and the current source I_s contain only the fundamental component they can be neglected at the harmonic frequencies. Based on Fig. 3, the harmonic component of grid current I_{g_h} introduced by V_h can be calculated as

$$I_{g_h} = \frac{I_{sa} Z_o Z_{oa} - V_h (Z_o + Z_{oa})}{Z_o Z_{oa} + Z_o Z_{L2} + Z_{oa} Z_{L2}} \quad (5)$$

For the analysis of the switching harmonic distribution of the high-power VSI, the high-power VSI is viewed as a switch mode voltage source while the impedance model of the auxiliary VSI is still applicable. The impedance model of the system at the sidebands of the switching frequency of the high-power VSI is shown in Fig. 4. In the figure, Z_{L1} is the impedance of the converter side inductor L_1 . The grid voltage V_h and V_s are neglected since they do not contain the frequency component. The switching behavior of the auxiliary VSI is neglected in this paper since its switching frequency is high and the dc-link voltage is low. Based on Fig. 4, the switching harmonics flowing into the grid $I_{g_{sw}}$ can be calculated as

$$I_{g_{sw}} = \frac{V_{sw} Z_{oa} + I_{sa} Z_{L1} Z_{oa}}{Z_{L1} Z_{oa} + Z_{L2} Z_{oa} + Z_{L1} Z_{L2}} \quad (6)$$

B. Harmonic Analysis and Control Targets

In order to ensure a sinusoidal output current I_g in the system shown in Fig. 1, both I_{g_h} and $I_{g_{sw}}$ should be zero. By solving (5) and (6), the requirements on I_{sa} and Z_{oa} can be obtained as follows:

➤ To ensure that I_{g_h} equals zero, the following equation should hold at the harmonic frequencies of the distorted grid voltage.

$$I_{sa} = V_h \left(\frac{1}{Z_o} + \frac{1}{Z_{oa}} \right) \quad (7)$$

Substituting (7) into the impedance model shown in Fig. 3,

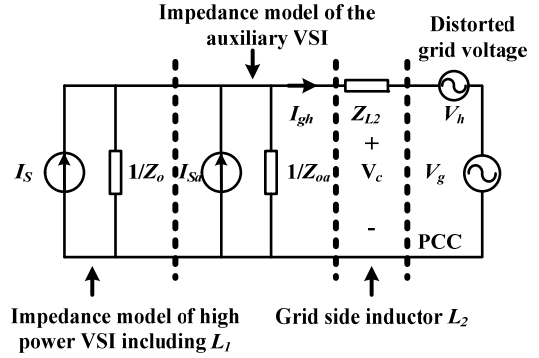


Fig. 3. Impedance model of the hybrid power system shown in Fig. 1 below the Nyquist frequency of the high-power VSI.

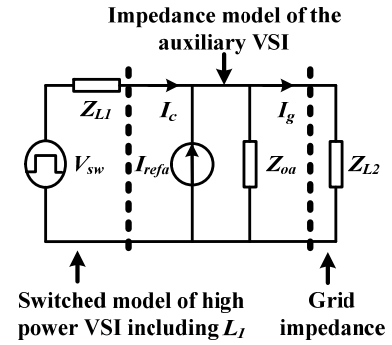


Fig. 4. System impedance model at the sidebands of the high-power VSI.

the converter side low-order harmonic I_{c_h} can be calculated as

$$I_{c_h} = -\frac{V_h}{Z_o} \quad (8)$$

➤ To ensure that $I_{g_{sw}}$ equals zero, the following equation should hold at the sidebands of the switching frequency of the high-power VSI

$$Z_{oa} (V_{sw} + I_{sa} Z_{L1}) = 0 \quad (9)$$

Substituting (9) into the impedance model shown in Fig. 4, the converter side switching ripple $I_{c_{sw}}$ can be calculated as

$$I_{c_{sw}} = \frac{V_{sw}}{Z_{L1}} \quad (10)$$

Equation (7) and (9) give the control objectives the auxiliary VSI. Equation (8) and (10) reveal the converter side distribution I_{c_h} of the harmonic currents when the grid current I_g is sinusoidal. From (8), it can be seen that when the grid side current I_g is free of the low order harmonics, all the harmonic voltage will be imposed on the converter side current I_{c_h} , and the magnitude of I_{c_h} is determined by the output impedance of the high-power VSI Z_o . Similar conclusion can be drawn for the switching harmonics $I_{c_{sw}}$.

III. HARMONIC MITIGATION OF GRID SIDE CURRENT I_g

A. Mitigation of the Low Order Harmonics Introduced by Grid Voltage

To eliminate the harmonics introduced by grid voltage, (7) and (8) should be met at the same time. Comparing (7) and (8), it can be found that the current source I_{Sa} is composed of two parts, the first part is the current response of the current control loop of the high-power VSI, and the second part is the current response of the auxiliary VSI itself. In other words, the current I_{Sa} should work in such a way that all the grid harmonic voltage V_h is imposed on the output impedance of the auxiliary VSI and the high-power VSI exclusively of the grid side inductor L_2 .

For the high-power VSI, the output impedance is determined by the impedance of L_1 and the gain of the current controller G_{cc} . With the low sampling frequency of the high-power VSI, it is difficult to design a current controller having a high gain near to the cross over frequency, which is roughly 1/6 of the sampling frequency. Thus, the impedance of Z_o is low at the harmonic frequencies. However, the output impedance of Z_{oa} at those frequencies can be very high, since the switching frequency of the auxiliary VSI can be much higher than the high-power VSI. With the high magnitude of Z_{oa} at the harmonic frequencies, the second term in (7) is close to zero and can be neglected. The current source should generate current in opposite with the converter side harmonics I_{c_h} . As a result, the auxiliary VSI should behave as a current source with high output impedance controlled by the harmonic current I_{c_h} . The working principle of I_{Sa} is given by (11) and the equivalent circuit is shown in Fig. 5.

$$I_{Sa} = I_{c_h} \quad (11)$$

B. Mitigation of the Switching Harmonics

To mitigate the switching harmonics of the high-power VSI, (9) and (10) should be met at the same time. Unlike the harmonic current introduced by the grid side harmonic voltage, the switching harmonics is introduced by the switch mode voltage source at the converter side. To realize (9), there are two options, which are given by (12) and (13), respectively.

$$I_{Sa} = -\frac{V_{sw}}{Z_{L1}} \quad (12)$$

$$Z_{oa} = 0 \quad (13)$$

For the first option given by (12), I_{Sa} should behave as a current source controlled by the converter side switching harmonic $I_{c_{sw}}$. However, the frequency of the switching harmonics is at the kilo Hertz level. For the normal operation frequency of the IGBT which is below 20 kHz, the sideband harmonics can reach the Nyquist frequency of the auxiliary VSI, which is beyond the achievable current control bandwidth. At the same time, (13) is much easier to be realized compared with (12). To realize (13) at a given frequency ω_i , G_{cca} should have a phase delay of 90 degrees, which can easily be done by using a Quadrature Signal Generator (QSG) at the sideband harmonic frequencies [5], [7]. In this manner, I_{refa} can simply be set to zero. The requirements of I_{refa} and G_{cca} at the i th sideband harmonic frequency ω_i are given by (14) and (15), respectively. The equivalent circuit is shown in Fig. 6, where the auxiliary VSI is 'short circuited' for the switching harmonics.

$$I_{refa} = 0 \quad (14)$$

$$G_{cca}(j\omega_i)G_{da}(j\omega_i) + jL_a\omega_i - j\frac{1}{C_a\omega_i} = 0 \quad (15)$$

It should be noted that the virtual impedance will not be perfectly realized with the digitally controller due to the discretization error, which will increase with lower sampling frequency. One way to reduce this error is to increase the sampling frequency. Also, the frequency for the impedance synthesizing is limited below the Nyquist frequency of the auxiliary VSI. Compared with the traditional method, the impedance based method has the draw-back of dependency on the accuracy of impedance. The advantages are:

- 1) The signal-to-noise ratio can be much higher for sensors measuring currents with low fundamental component;
- 2) Tuning of the current controller is simple and there is no need to calculate the current reference, which simplifies the design procedure and reduces the computational burden.

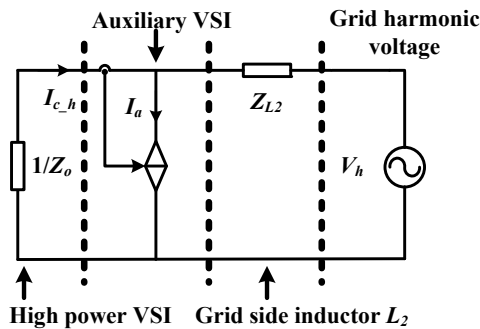


Fig. 5. Impedance model of the system with the auxiliary VSI controlled to meet (11).

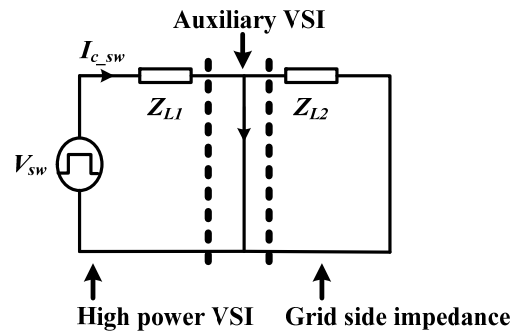


Fig. 6. Impedance model of the system with the auxiliary VSI is controlled to meet (14) and (15).

C. Impacts of the Grid Impedance

For the low-order harmonics introduced by the grid voltage, the auxiliary VSI ensures that the grid side $I_{g,h}=0$ by meeting (11). The converter side harmonics can be then calculated by (8), indicating that the background harmonics are virtually moved to the terminal of the converter side inductor regardless of the grid impedance. Since the grid impedance originally helps with sharing the harmonic voltage, there will be an increase in the converter-side low-order harmonics and the compensating current from the auxiliary VSI. In the design phase of the auxiliary VSI, the largest grid impedance should be considered to dimension the auxiliary VSI. For the switching harmonics, the inductive grid impedance helps to force the switching harmonics into the auxiliary VSI. However, parallel capacitance in the grid, even though often neglected, can introduce parallel resonance with the grid side inductor L_2 . If the parallel resonance frequency falls in the vicinity of the switching harmonics, the grid capacitance will also absorb the switching ripples of the high power VSI.

IV. CONTROL SYSTEM DESIGN OF THE AUXILIARY VSI

Based on the analysis in § I and § III, there are three control targets for the control system of the auxiliary VSI, the first one is tracking of the current reference $I_{c,h}$ at the low order harmonics, the second one is providing zero output impedance at the sideband frequencies and the last one is to maintain the dc-link voltage. The resultant overall control system of the auxiliary VSI is shown in Fig. 7. There are three control loops, namely the Active Trap Filtering (ATF) loop, the Active Power Filtering (APF) loop, and the dc-link voltage control loop. The ATF loop is responsible to mitigate the switching harmonics, the APF loop is responsible for mitigating the lower order harmonics and the dc-link voltage is responsible to maintain the dc-link voltage of the auxiliary VSI. The system parameters under study are listed in Table I.

A. ATF Loop

The ATF loop re-shapes the output impedance of the ATF at the dominating sidebands of the switching harmonics of the high-power VSI. To achieve the zero output impedance Z_{oa} ,

TABLE I.

Electrical Parameters of the Studied System.

Block	Parameter	Value
High-power VSI	Switching frequency f_{sw}	2 kHz
	Converter side inductor L_c	5 mH
	Grid side inductor L_g	1.5 mH
	dc-link voltage V_{dc}	730 V
Active Trap Filter (ATF)	Switching frequency f_{swt}	20 kHz
	Filter inductor L_t	1.5 mH
	Filter capacitor C_t	10 μ F
	dc-link voltage V_{dct}	200 V

the current controller G_{ATF} is composed of QSGs connected in parallel. The QSGs will introduce frequency selective virtual capacitance, which can be used to artificially introduce series resonance with the passive LC filter at the targeted frequencies ω_i . Since the time delay $G_d = e^{-1.5T_d s}$ introduces phase lag at ω_i , the QSGs should provide phase compensation. The expression for G_{cca} is given by (16) and (17) [17].

$$G_{ATF}(s) = \sum K_i G_{QSGm}(s) \quad (16)$$

$$G_{QSGm}(s) = \frac{2\omega_c \sin(\alpha)s + 2\omega_c \omega_i \cos(\alpha)}{s^2 + 2\omega_c s + \omega_i^2} \quad (17)$$

where ω_c is the bandwidth of the QSG and α is the compensation angle. At ω_i , the QSG and G_{da} can be replaced with the operator $-j$. At other frequencies, the impact of the QSG can be neglected. To achieve zero output impedance at ω_i , K_i can be calculated by

$$K_i = \omega L_i - \frac{1}{\omega C_i} \quad (18)$$

The impedance characteristic of Z_{oa} around the sideband harmonics is shown in Fig. 8. The magnitude of Z_{oa} is close to zero at the sideband harmonic frequencies. In other words, condition (13) is met and the switching ripples will be bypassed by the auxiliary VSI.

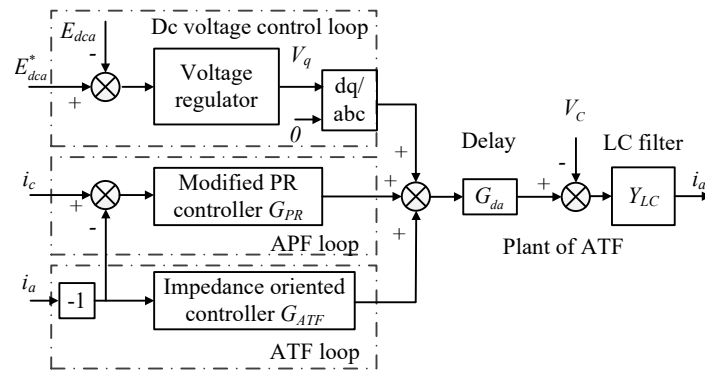


Fig. 7. Overall control structure of the auxiliary VSI.

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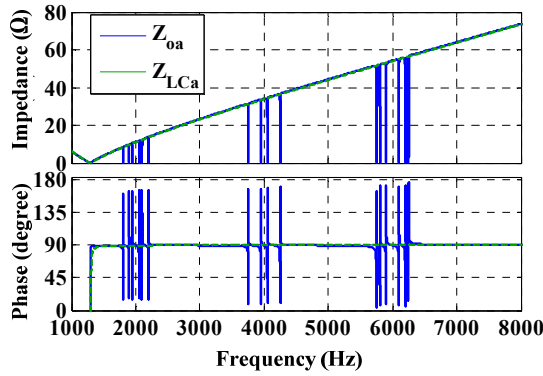


Fig. 8. Frequency characteristic of output impedance Z_{0a} above the Nyquist frequency of the high-power VSI.

B. APF Loop

The APF loop is shown Fig. 7, where the reference I_{refa} is set to the harmonic component of the converter side current I_c and a Proportional and Resonant (PR) controller is used as the current controller. The R controller increases the open loop gain at its resonant frequency and the P controller determines the cross over frequency where the open loop gain is zero dB. Since the P controller does not have frequency selectivity, it will interact with other control loops. To solve this problem, notch filters are connected in series with the P controller. The notch frequencies should include the fundamental frequency and the sideband harmonic frequencies. Since the sideband frequencies and the low order harmonic in the grid voltage are separated in the frequency domain and the gains of the notch filters are close to unit beyond the notch frequencies, they can be neglected for the design of the APF loop. The detailed structure of the modified PR controller is shown in Fig. 9.

At the resonant frequencies of the R controllers, the closed loop gain becomes unity and the output impedance Z_{0a} is high and can be viewed as open circuit. At other frequencies, the output impedance cannot be viewed as open circuit. Denote the closed loop gain of the auxiliary VSI by G_{cla} , which is given by (3), the impedance model of the system is shown in Fig. 10. From the figure, it can be seen that the auxiliary VSI has two effects on the output impedance of the system:

- Output impedance of the high-power VSI is increased from Z_o to $Z_o/(1-G_{cla})$, which means that the high-power VSI is more robust to the distortion of the grid voltage.
- The P controller of the auxiliary introduces virtual resistance in to Z_{0a} , whose expression is given by (19), hence the system is better dampened with the auxiliary VSI.

$$R_{da} = K_{pa} e^{-1.5T_{sa}s} \quad (19)$$

The total output impedance of the system can be obtained by

$$Z_{ot} = \frac{Z_o Z_{0a}}{Z_o + (1 - G_{cla}) Z_{0a}} + Z_{L2} \quad (20)$$

With the control parameters shown in Table II, the calculated and simulated frequency characteristics of $Z_o + Z_{L2}$ and Z_{ot} are shown in Fig. 11 when R controller is tuned at 13th harmonic. From the figure, it can be seen that the magnitude characteristic matches well between the simulation and the calculation, however there is error between the phase calculations. In area A in Fig. 11, the auxiliary VSI increases the output impedance of the system, especially at the resonant frequency of the R controller. In area B, the auxiliary VSI decrease the output impedance. Above 300 Hz, the simulated output impedance Z_{ot}

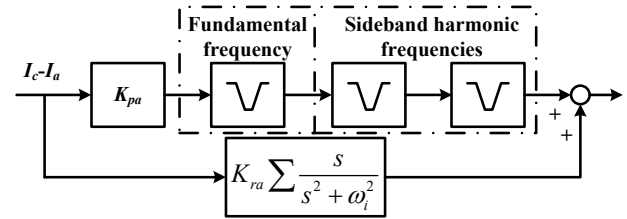


Fig. 9. PR controller with modified proportional term in Fig. 7.

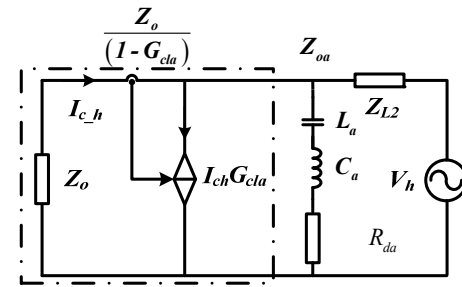


Fig. 10. General impedance model of the system when the output impedance of the auxiliary VSI is not neglected.

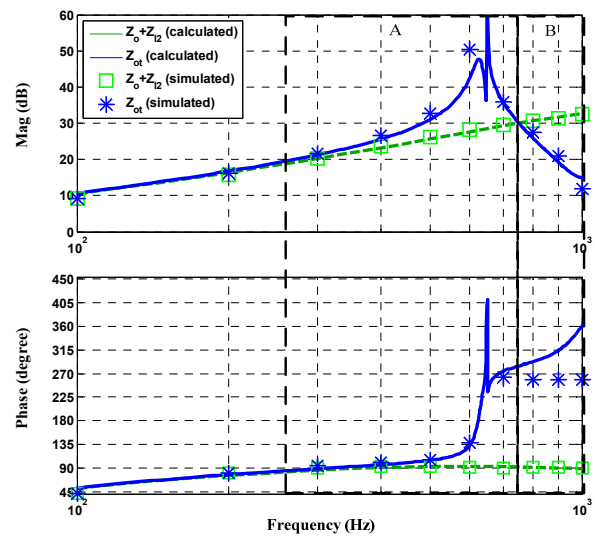


Fig. 11. Frequency characteristics of output impedance Z_o above the Nyquist frequency of the high-power VSI.

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TABLE II
Control Parameters of the System.

Block	Parameter	Value
Auxiliary VSI	K_{pa}	2
	K_{ra}	500
High-power VSI	K_p	4
	K_r	1000

has a phase angel between 90 and 270 degrees, indicating a negative real part. Below 600 Hz, the system shows impedance characteristic of negative resistance and inductance; above 700 Hz, the system shows impedance composed of negative resistance and capacitance. Hence the system is sensitive to capacitive grid admittance below 600 Hz and inductive grid admittance above 700 Hz.

C. DC-link Control Loop

As shown in Fig. 7, the output of the dc-link voltage regulator is fed to the q -axis of the output voltage. The d -axis component is set to zero. With this configuration, the active power of the auxiliary VSI is calculated to be

$$P = V_{oa} I_{g0} \quad (21)$$

where

$$I_{g0} = \omega_f V_s C_a \quad (22)$$

The closed loop control diagram is shown in Fig. 12. Ideally, the closed loop system becomes a first order system with a P controller. In practical applications, the parasitic resistance will introduce some steady state error. In order to remove the steady state error, an Integral (P) controller should be used, with which the closed loop system becomes a second order system. Denote the proportional gain with K_{p_dc} and the integral gain with K_{i_dc} , the closed loop transfer function of the dc-link control loop can be obtained as

$$G_{cl_dc} = \frac{2\xi\omega_{dc}s + \omega_{dc}^2}{s^2 + 2\xi\omega_{dc}s + \omega_{dc}^2} \quad (23)$$

where

$$\omega_{dc} = \sqrt{K_{i_dc} I_{g0}}, \quad \xi = 2K_{p_dc} \sqrt{\frac{I_{g0}}{K_{i_dc}}} \quad (24)$$

are the natural frequency and damping ratio of the dc-link control loop, respectively. By setting the damping ratio ξ to the typical value of 0.707 and the bandwidth to ω_{b_dc} , the control gains can be obtained as (25) and (26), respectively. In this paper, ω_{b_dc} is set to 10 rad/s.

$$K_{p_dc} = \frac{0.47\omega_{b_dc}}{I_{g0}} \quad (25)$$

$$K_{i_dc} = \frac{0.23\omega_{b_dc}^2}{I_{g0}} \quad (26)$$

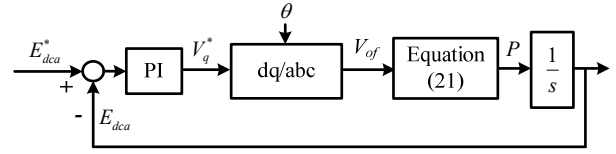


Fig. 12. Closed loop control of dc-link voltage.

V. SIMULATION RESULTS

The parameters of the simulated system are shown in Table I and Table II. The 13th harmonic is injected in to V_g while other harmonics like the 5th and 7th can be injected as well. Since 13th harmonic is out of the current control bandwidth of common high-power VSIs, only 13th harmonic is injected. Other harmonics can be compensated by the APF loop in the same manner. The waveforms of V_g , I_g , I_c and I_a with both ATF and APF loop enabled are shown in Fig. 13. The grid current I_g is sinusoidal while the converter side current I_c is distorted heavily by the switching harmonics and the low order harmonics introduced by V_h . All the switching and low order harmonics are bypassed by the auxiliary VSI through I_a .

To show the performance of the ATF loop clearly, V_h is removed and the waveforms of I_g and I_a before and after enabling the ATF loop are shown in Fig. 14(a) and Fig. 14(b), respectively. When the ATF is enabled, switching harmonic in I_g is decreased while the switching harmonics in I_a is increased. To show the performance of the APF loop, the waveforms of I_g and I_a without enabling the APF loop are shown in Fig. 15(a) and Fig. 15(a), respectively. When the APF loop is not enabled, low order harmonics appear in the I_g .

The waveforms of I_g and I_a during the step change of the current reference I_{ref} of the high-power VSI is shown in Fig. 16. As it can be seen, there is no abrupt change in I_a which indicates that the auxiliary VSI does not influence the dynamic performance of the high-power VSI. The performance of the dc-link control loop is shown in Fig. 17, where the dc-link voltage is stepped down from 400 V to 200 V. It takes 0.8 s to enter the steady state.

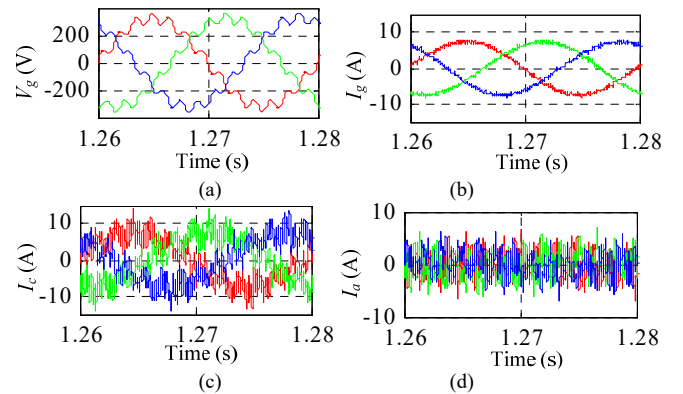


Fig. 13. Simulated steady state waveforms of V_g , I_g , I_c and I_a . (a). Waveforms of V_g . (b). Waveforms of I_g . (c). Waveforms of I_c . (d). Waveforms of I_a .

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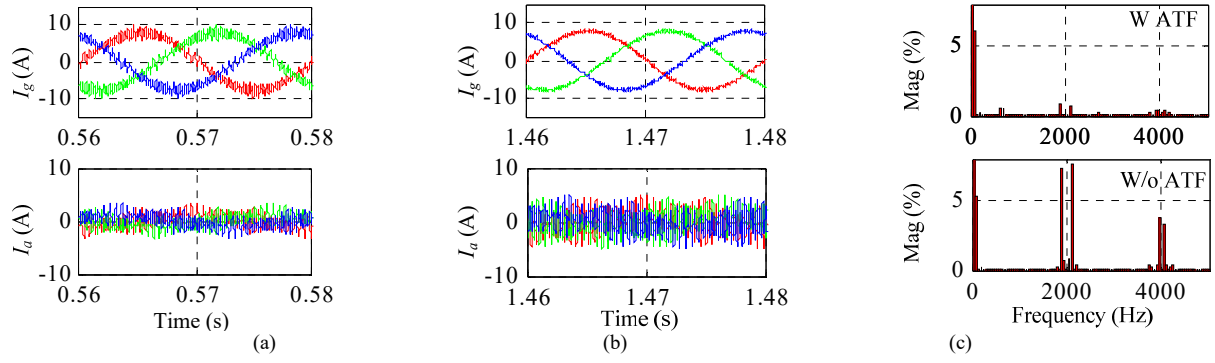


Fig. 14. Simulated waveforms of I_g and I_a with / without the ATF loop. (a). Waveforms of I_g and I_a when the ATF loop is not enabled. (b). Waveforms of I_g and I_a when the ATF loop is enabled. (c). FFT comparison w and w/o ATF loop.

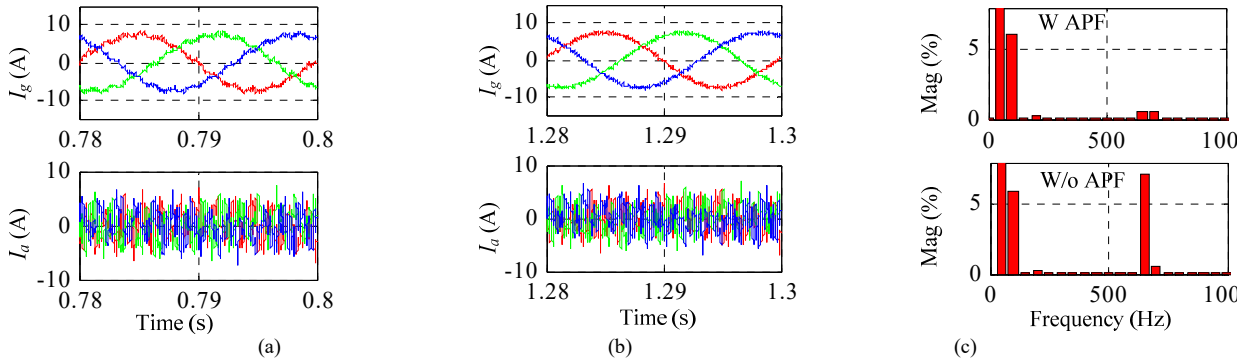


Fig. 15. Simulated waveforms of I_g and I_a with / without the APF loop. (a). Waveforms of I_g and I_a when the APF loop is not enabled. (b). Waveforms of I_g and I_a when the APF loop is enabled. (c). FFT comparison w and w/o APF loop.

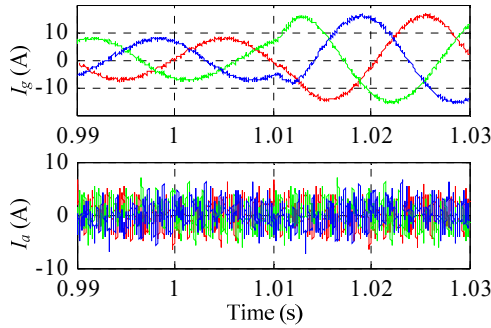


Fig. 16. Simulated waveforms of I_g and I_a when I_{ref} increased.

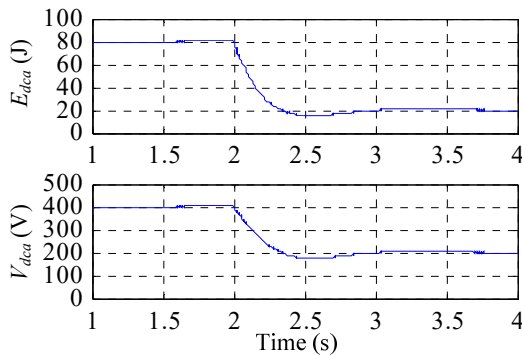


Fig. 17. Simulated waveform of V_{dca} with a step change of V_{dcrefa} .

VI. EXPERIMENTAL RESULTS

A programmable AC source is used as the grid voltage. The 13th harmonic is injected into V_g to represent the background harmonic voltage. When the auxiliary VSI is not connected, the waveforms of V_g , I_g , I_c and I_a are shown in Fig. 18. As it can be seen, I_g contains not only the switching harmonic but also the low order harmonics introduced by the grid voltage. When the auxiliary VSI is connected to the system, the waveforms of V_g , I_g , I_c and I_a are shown in Fig. 19. Both the switching harmonics and the low order harmonics are compensated by the auxiliary VSI. The magnitude of $I_{c,h}$ is increased as expected. The transient performance when the reference for the high-power VSI I_{ref} stepped from 4 A to 7 A is shown in Fig. 20. During the transient process, there is no abrupt change in I_a , indicating that the control of the auxiliary VSI and the high-power VSI are decoupled from each other. The dynamic performance of the high-power VSI is not depreciated by the auxiliary VSI.

In order to show the performance of the ATF loop clearly, the grid harmonic voltage is removed. The waveforms of V_g , I_g , I_c and I_a before and after enabling the ATF loop is shown in Fig. 21 and Fig. 22, respectively. The suppression of the switching harmonics is about 6 dB up to 6 kHz and about 15 dB for 8 kHz. The details are summarized in Table III. The performance of the ATF is comparable with the conventional current-injecting method. The transient performance when the

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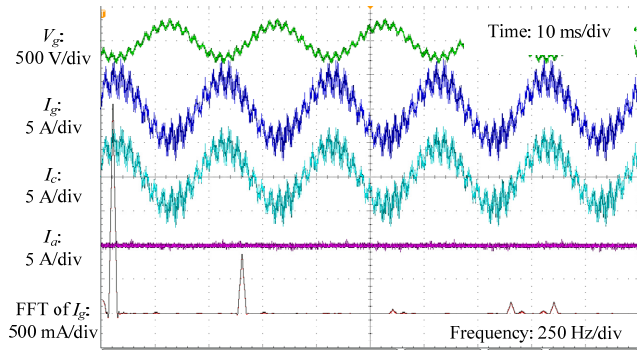


Fig. 18. Waveforms of V_g , I_g , I_c and I_a in when grid voltage is distorted and the auxiliary VSI is not connected.

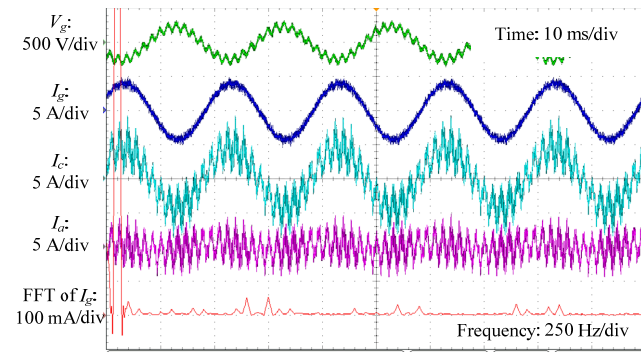


Fig. 19. Waveforms of V_g , I_g , I_c and I_a in steady state when grid voltage is distorted and the auxiliary VSI is connected with the ATF and APF loop enabled

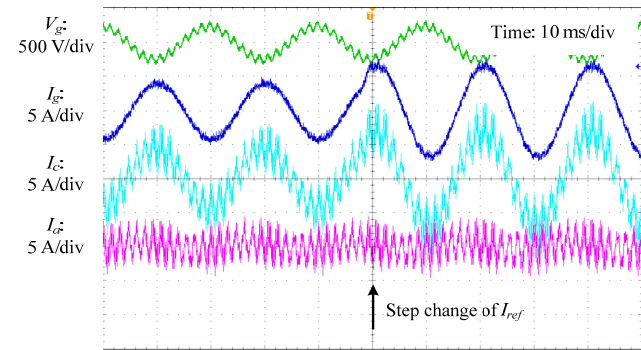


Fig. 20. Waveforms of V_g , I_g , I_c and I_a during the step change of I_{ref} .

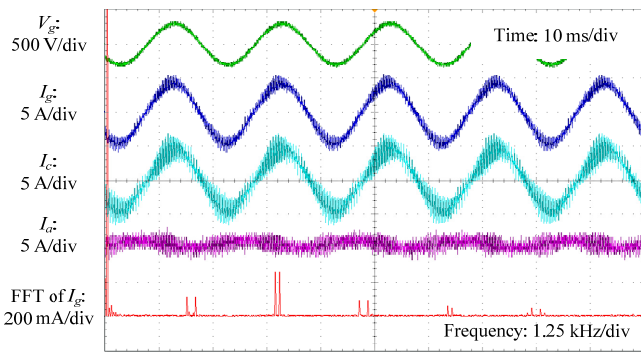


Fig. 21. Waveforms of V_g , I_g , I_c and I_a in steady state when ATF loop is disabled and grid harmonic voltage is sinusoidal.

TABLE III
HARMONIC MAGNITUDES OF I_g

Control loop	State	13 th	2 kHz	4 kHz	6 kHz	8 kHz
ATF loop	disabled	-	2.4%	5.2%	2%	1.2%
	enabled	-	1%	2.6%	0.8%	0.2%
APF loop	disabled	17.4%	-	-	-	-
	enabled	1%	-	-	-	-

ATF loop is enabled is shown in Fig. 23. It takes about 0.12 s for the ATF loop to enter into steady state.

In order to show the performance of the APF loop, the waveforms of I_g , V_g , I_c and I_a are shown in Fig. 24 when the 13th harmonics is injected into V_g and the APF loop is disabled. As it can be seen, I_g is heavily distorted with the 13th harmonics. When the APF loop is enabled, the waveforms have already been shown in Fig. 19. Comparing between Fig. 19 and Fig. 24, it can be seen that the magnitude of 13th harmonic in I_c is increased as expected. The magnitudes of 13th harmonic in I_g before and after enabling the APF loop are summarized in Table III. The transient performance when the APF loop is enabled is shown in Fig. 25 and it takes about 0.15 s for the APF loop to enter the steady state. The performance of the dc-link control loop is shown in Fig. 26, where the reference for the dc-link voltage is stepped down from 400 V to 200 V. The steady state error is small and the dynamic process takes 0.6 s.

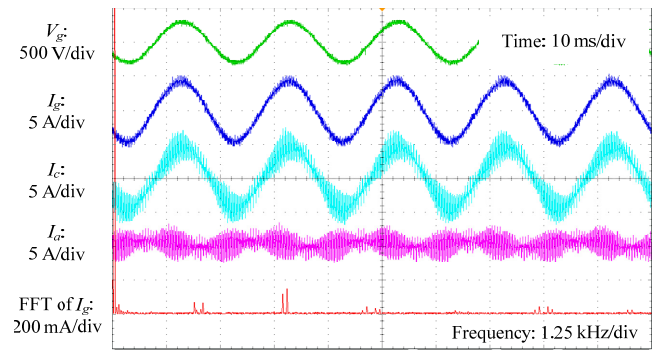


Fig. 22. Waveforms of V_g , I_g , I_c and I_a in steady state when ATF loop is enabled and grid harmonic voltage is sinusoidal.

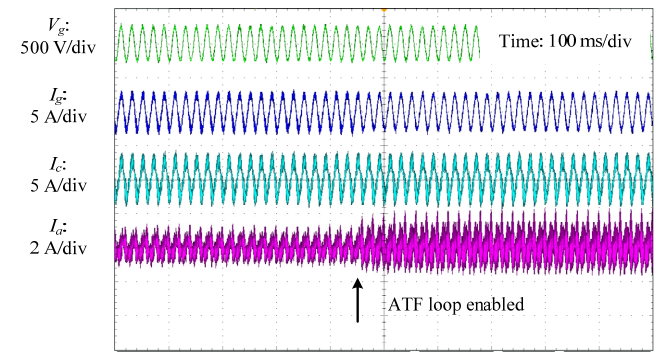


Fig. 23. Waveforms of V_g , I_g , I_c and I_a during the transient process when the ATF loop is enabled.

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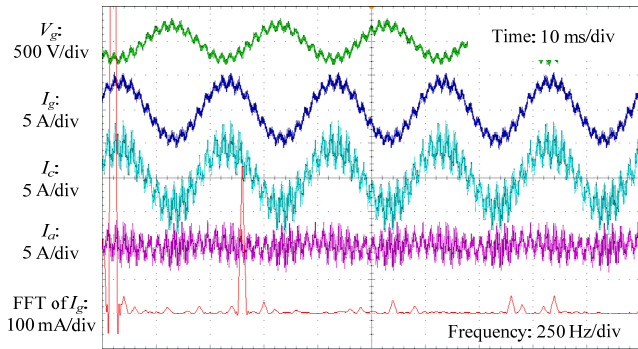


Fig. 24. Waveforms of V_g , I_g , I_c and I_a when grid voltage is distorted and the APF loop is disabled.

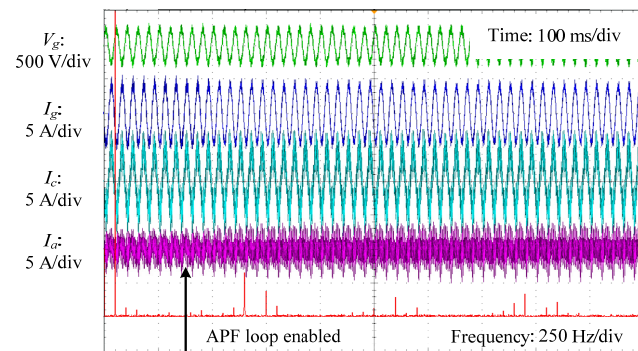


Fig. 25. Waveforms of V_g , I_g , I_c and I_a during the transient process when the APF loop was enabled.

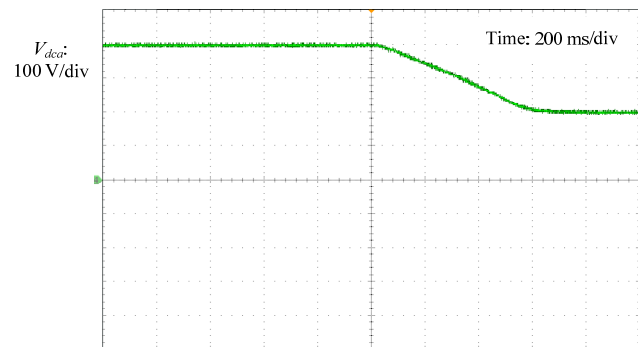


Fig. 26. Waveform of V_{dca} when the reference is stepped from 400 V to 200 V.

VII. CONCLUSIONS

In this paper, the control strategy of the auxiliary VSI in the system shown in Fig. 1 is developed to mitigate both the switching harmonics and the low order harmonics. In order to derive the requirements of the control system, impedance model of the system is built to analyze the harmonic interaction. The following facts are revealed: to eliminate the impact of the distorted grid voltage, the auxiliary VSI should track the converter side harmonics; to mitigate the switching harmonics, the output impedance of the auxiliary VSI should be close to zero at the sideband frequencies. The dc-link voltage of the auxiliary VSI is maintained by a PI controller along the q -axis. Simulation and experimental results show

that the proposed control system is effective. The proposed control method might be of interest for future high power VSI to meet more stringent harmonic requirements.

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